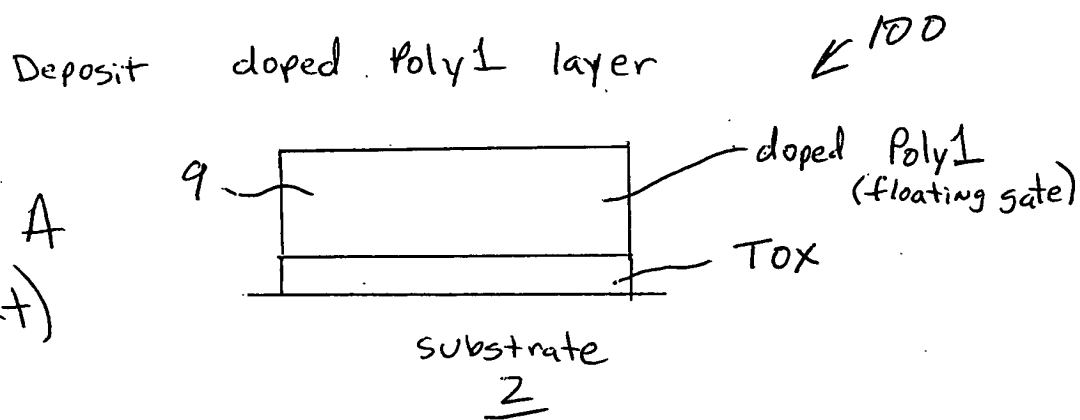
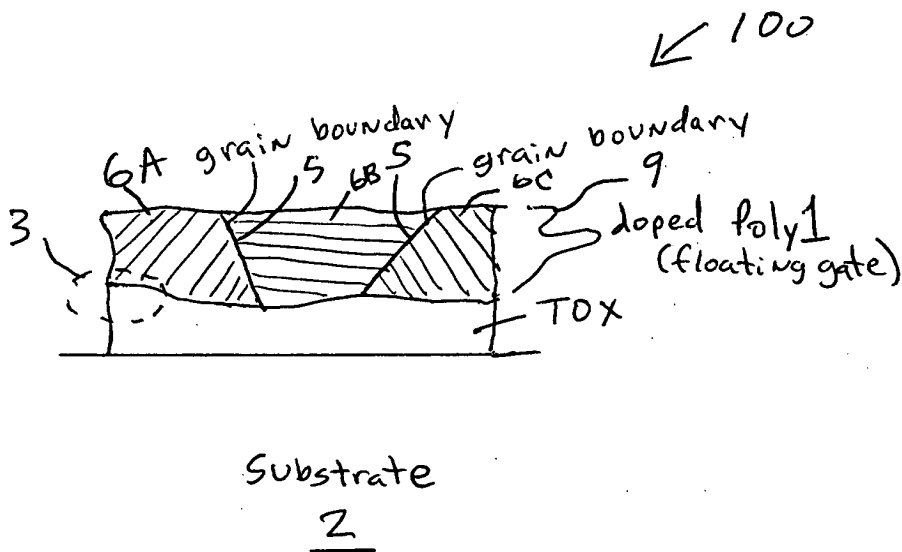


Figure 1 A
(prior Art)



after thermal processes have been performed

Figure 1 B
(Prior Art)



Poly2 (control gate)

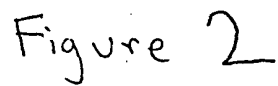


Figure 2

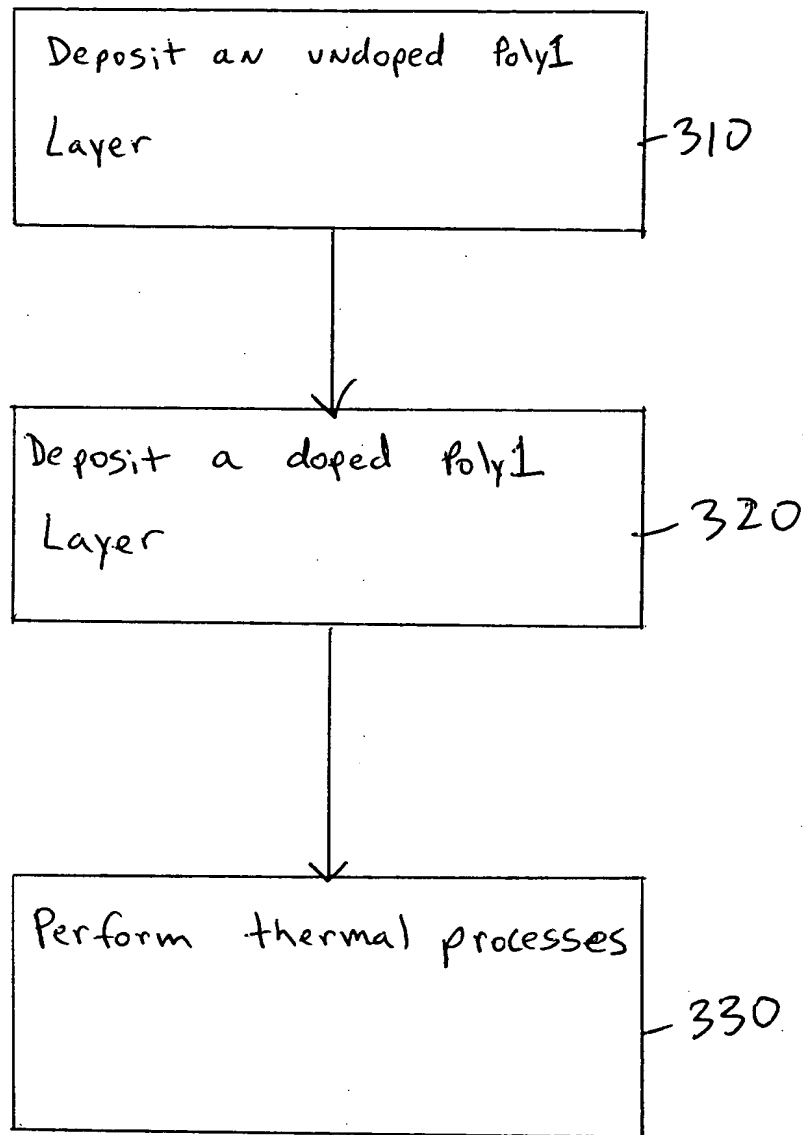
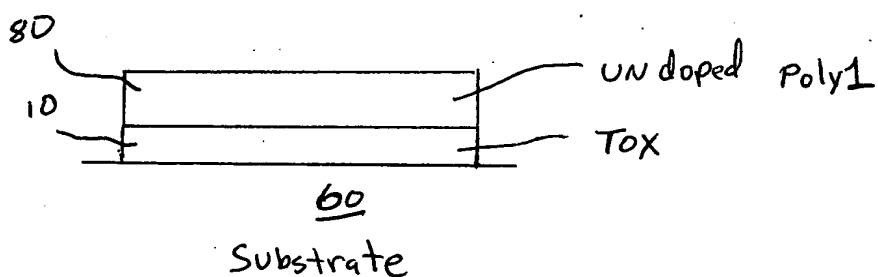


Figure 3

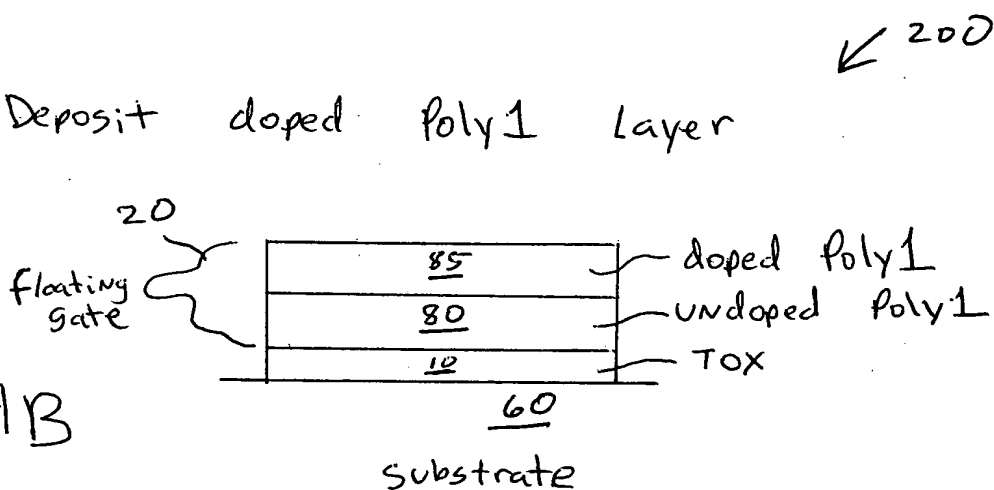
↙ 200

Figure 4A



Deposit doped Poly 1 Layer

Figure 4B



After thermal processes have been performed

Figure 4C

